ABSTRACT

[0078] An FPGA architecture has top, middle and low levels. The top level is an array of B16xl6 tiles enclosed by I/O blocks. The routing resources in the middle level are expressway routing channels including interconnect conductors. At the lowest level, there are block connect routing channels, local mesh routing channels, and direct connect interconnect conductors to connect the logic elements to further routing resources. Each Bl block includes four clusters of devices. Each of the clusters includes first and second LUT3s, a LUT2, and a DFF. Each of the LUT3s have three inputs and one output. Each of the LUT2s have two inputs and one output. Each DFF has a data input and a data output. In each of the clusters the outputs of the LUT3s are multiplexed to the input of DFF, and symmetrized with the output of the DFF to form two outputs of each of the clusters.